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54 **Amplifier for radio transmitter having controllable output power.**

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the output power with and without attenuation in an accurate attenuator. By this means, a wide adjustment of output power is possible over a narrow range of measured power.

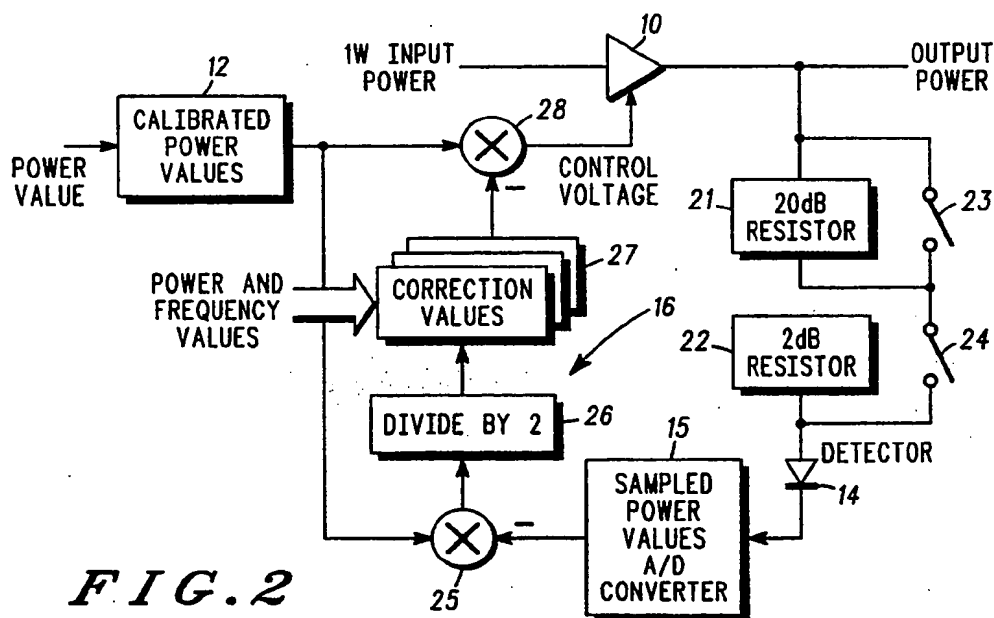


FIG. 2

AMPLIFIER FOR RADIO TRANSMITTER HAVING CONTROLLABLE OUTPUT POWER

Background of the Invention

This invention relates to a power amplifier for a radio transmitter having accurately controllable output power suitable for use in cellular radio base stations, particularly for the Pan-European GSM network.

The GSM specification requires that a base station's transmitter has a predetermined maximum output power having a tolerance of -0 or +3dB and may be reduced from its maximum level in up to 21 steps of 2dB with an accuracy of + or -0.5dB.

The specification is a very demanding one, because, whereas control of output power to a tolerance of + or -0.5dB at a particular power level and frequency is possible, achievement of this tolerance at any level over a range of 42dB and over a range of frequencies is a requirement not heretofore seen. The set requirement is even more difficult to achieve when the transmitter is hopping from one frequency to another and from one power level to another between time slots, where each time slot lasts for only 577 microseconds.

It is an object of the present invention to provide a transmitter which meets the required specification and is simple, cheap and reliable.

Summary of the Prior Art

EP-A-0369135 of Motorola Inc. describes a power amplifier for a radio frequency signal utilizing a microprocessor to address a read-only memory (ROM) to look up a power control value for setting the output power of an RF power amplifier. That amplifier is particularly suitable for meeting the less stringent requirements of the specification for mobile cellular radio transmitters. The output power is measured by means of a detector diode. It is a problem that output power detectors cannot readily measure output power accurately over a power range as great as 42dB. On the contrary, production tolerance and batch tolerance in detector diodes can give rise to a variance of 3-4dB at the extremes of the power range.

Summary of the Invention

According to the present invention, there is provided an amplifier comprising a controllable output power stage, power setting means for setting the output power, and a control loop for adjusting the output power, the control loop comprising measuring means for measuring the output power and

comparison means for comparing the power measured with the power set and adjusting the output power in response thereto, characterised by attenuator means switchable into the control loop for causing the measuring means to measure attenuated power, storage means for storing a value for measured power and means for storing a stored value derived from a first switched state of attenuation for adjustment of the output power during a second switched state of attenuation, thereby to allow a wide adjustment of output power over a narrow range of measured power.

By this means, only a single setting of the output power needs to be made in the factory, or by a service engineer, and using this reference power, a highly accurate but cheap attenuator, such as a laser etched resistor pad, can be used to provide calibration for other power levels.

The transmitter can perform an automatic calibration routine, which results in a number of reference values stored in memory, each controlling an output power level to a high degree of accuracy.

There is preferably provided a large attenuator and a small attenuator and switching means for switching one or both of said attenuators into the control loop. By this means, the entire power range can be divided up into smaller steps, equivalent to the power attenuation provided by the small attenuator, while the large attenuator can provide power control equal to a number of smaller steps, thus reducing the total number of steps required to span the entire power range.

According to the invention there is also provided a method of controlling the output power of an amplifier, comprising the steps of:

- a) setting an output power stage to provide a desired higher output power, attenuating the output power in an attenuator, and measuring and storing a value for the attenuated output power
- b) deactivating the attenuator and
- c) adjusting the setting of the output power stage until substantially the same output power value is measured as the stored value, thereby providing a decreased output power, the value of which is controllable to substantially the same degree of accuracy as the measurement of the previously attenuated higher output power.

In this manner a higher power level is set in the factory, by a service engineer, or by other means, and, using this higher power level as a reference point, further (lower) power levels are calibrated by the transmitter itself in a two-stage process of power measurement with attenuation and power measurement without attenuation.

A reverse procedure may be used in which a

lower power level is set initially and a two-stage calibration is performed by measurement without attenuation and measurement at a higher power with attenuation.

It is preferred that both methods are used and the calibration results are averaged.

A further stage of calibration may be used, in which output power is set to different levels extending over a range by a series of steps including at least one large incremental step in one direction and a series of small incremental steps in the other direction. If the final power level is found to be different to the original level (e.g. due to non-linearity in the amplifier), interpolation may be used to adjust the stored values for the intermediate small incremental steps, so as to equalise the final level to the originally measured level.

Brief Description of the Drawings

Figure 1 illustrates two methods of power control in accordance with the invention;

Figure 2 shows a block diagram of a power amplifier in accordance with a preferred embodiment of the invention;

Figure 3 shows a graph of detector value versus control voltage for the amplifier of Figure 2; and Figure 4 shows preferred details of the attenuators and detector of figure 2;

Figure 5 shows preferred details of the portion of figure 4 in dotted outline; and

Figure 6 shows an alternative arrangement for the detector of Figure 2.

Detailed Description of a Preferred Embodiment

Referring to Figure 1, there are shown two methods of power control in accordance with the invention, illustrated in Figures 1a and 1b respectively.

In Figure 1a, there is shown a power amplifier 10 having a gain input 11 and means 12 for setting the gain input. There is also shown an attenuator 13, a detector 14, storage means 15 and control means 16.

The figure has three parts, representing the steps in the method. The first and second parts in fact represent steps performed simultaneously, while the third part represents a subsequent step.

The operation of the amplifier is as follows. A value is provided by setting means 12, which provides a control voltage on the input 11 of the power amplifier 10, which results in a high power output at the output of the amplifier. The value is pre-calibrated, so that the high output power is accurate to within the desired specification. The output power may be, for example, 80 watts.

As shown in step II, the output power is attenuated in the attenuator 13 to a low power level. The attenuator may provide, for example, 20dB attenuation. The low power level resulting is measured by detector 14, and the value is stored in storage means 15 in order to record the measured power level. In step III, this stored value is recalled and the control means 16 ramps up the control voltage to the power amplifier from zero volts until the output power level measured by the detector 14 without any attenuation is equal to the value stored in step II.

In an alternative method, illustrated in Figure 1b, which may be considered the opposite to the above method, the initial power level set by setting means 12 is a low power level, and the measured value is stored in storage means 15. The attenuator 13 is then switched into the circuit between the output of the power amplifier and the detector 14, and the control means 16 increases the gain of the amplifier, until the measured power value is equal to the stored value.

In each of the cases illustrated in Figures 1a and 1b, it may be noted that the detector 14 always detects the lower power value. Thus, the output power is controllable over a range substantially greater than the range of effective accurate measurement of the detector 14.

It will be appreciated that there does not need to be a linear relationship between the control voltage on amplifier control input 11 and the power measured by detector 14.

Referring to Figure 2, more detailed apparatus is shown for implementing the method of Figure 1a. In this figure, the attenuator means is shown to comprise a 20dB laser trimmed resistor pad 21 and a 2dB pad 22, each having a bypass switch, 23 and 24 respectively. The switches enable both pads to be connected in series, to provide their combined attenuation. The storage means 15 is an analog-to-digital converter providing digital power values to the memory of a microprocessor (not shown). The control means 16 is shown as comprising a comparator 25, a divider 26, frequency correction means 27 and a subtractor 28. These components can all be implemented in software and the resultant output of subtractor 28 can be converted to analogue form for controlling the power amplifier 10.

In general terms, the setting means 12 provides a series of calibrated power values, the derivation of which is described below. The circuit elements 25 to 28 facilitate power control during use, to equalise the output power to the desired power level. It will be appreciated that, because the output power level changes from one time slot to the next, the control loop provided does not control the output power instantaneously, but utilises pre-

viously measured power levels to control forthcoming time slots.

Calibration

The maximum output power value is set manually, by adjusting the control voltage to the power amplifier 10, until the output power is measured to be the desired maximum level (e.g. 80 watts) using highly accurate calibration equipment. The voltage V_{22} applied to the control input of the amplifier to provide this measured power is recorded in setting means 12. Thereafter, calibration is fully automatic and is carried out by a calibration routine stored in the microprocessor of the transmitter. This routine is now explained with reference to Figure 3.

The following steps are carried out.

(a) The 20dB pad 21 is switched into the detector circuit by opening switch 23 (with switch 24 closed.)

(b) The power amplifier is set to maximum power (80 watts), by recalling the calibrated power value V_{22} from setting means 12.

(c) The resulting power value D_{12} at the detector 14 is measured and stored in storage means 15.

(d) The control voltage V_N is decreased to zero and the 20dB pad is switched out of the circuit by closing switch 23.

(e) The control voltage to the power amplifier is increased from zero until the value D_{12} stored in step (c) is detected at the detector 14.

(f) The control voltage V_{12} required for step (e) is stored (the mid power value).

(g) The 20dB pad 21 is switched into the circuit again.

(h) Using the mid power control voltage V_{12} , the value D_2 measured by the detector 14 is stored.

This is near the low point of the detector.

So far, only three control voltages have been stored, these being numbers V_{22} , V_{12} and V_2 on Figure 3. In addition, two detector values have been stored D_{12} and D_2 .

The next stage in the procedure is to find control voltages for intermediate power levels between the maximum power and the mid power values V_2 and V_{12} , at 2dB intervals.

(i) With 20dB pad 21 switched out of the detector circuit, the 2dB pad 22 is switched in by opening switch 24.

(j) The control voltage is increased from zero to give the last detector value (the low point).

(k) The control voltage V_3 is stored.

(l) The 2dB pad is switched out by closing switch 24.

(m) The detector value D_3 is measured and stored.

Steps (i) to (m) are repeated, in each case

using the last measured detector value and increasing the voltage with attenuation on the output until that detector value is achieved. In this manner, the various values V_3 - V_{11} and D_3 - D_{11} on Figure 3 are measured and stored.

(n) Having read ten sequential pairs of detector values and control voltages, it is possible to check the difference between the last pair of values and the values D_{12} and V_{12} read in steps (c) and (e). If there is a difference, the values read in steps (i) to (m) are interpolated to fit the previously measured range, i.e. to equalise the final measured values and the initially measured values. Interpolation has the effect of increasing or decreasing the incremental step between power control voltage values and/or the step between detector values. Having finally interpolated the values, they can be stored in read-only memory in setting means 12 and are thereafter available for use during transmitter operation.

Having read the detector values and control values for the steps 2 to 12 of the 42dB dynamic range, the next stage is to use the same detector values for the upper 2dB steps to read the control voltages. This is done as follows:

(o) Select the control voltage V_{12} read in step (h);

(p) With the 20dB pad 21 switched into the detector circuit, the 2dB pad is switched out.

(q) The control voltage is increased from zero until each of the detector values D_2 to D_{12} is reached in turn. At each value, the control voltage is stored. This gives the values V_{13} - V_{21} and also a repeat value for V_{22} .

(r) Values V_{13} - V_{21} are adjusted by linear interpolation so as to equalize the repeat value for V_{22} with the originally set value (as for step n).

So far, twenty-one power control values and eleven detector values have been stored. The single remaining necessary pair of values is obtained by selecting V_2 , measuring the detector value D_1 with both pads 21 and 22 switched in to the circuit, bypassing pad 22 and dropping the control voltage to the level V_1 at which detector value D_1 is measured. (Of course, if pad 21 had a greater value, e.g. 22dB, this step would be unnecessary, but an extra step in the sequence (a)-(r) would be required).

Upon completion of the calibration routine, a full table of twenty-one 8-bit control voltage values is stored in setting means 12.

It will be noted from Figure 3 that the upper half of the detector's range, from D_{12} to D_{MAX} , is never used. Hence a detector can be used that has much less dynamic range. Also, the control voltage is always reduced to zero before bypassing either attenuator, so as not to exceed the detector's maximum power rating.

Control During Operation

In order to correct for temperature, drift and frequency variations within the amplifier, a correction table is updated for each timeslot.

During operation, a required power level is selected by calling up the appropriate calibrated power value from setting means 12. With each time slot of transmission output, the output power is detected by detector 14 and sampled by the A/D converter in sample and storage means 15. If the output power is within the upper half of the range (as determined by the power level being selected), pad 21 is switched into the circuit, otherwise pad 21 is bypassed by switch 23. The detector value is translated into a control voltage error (by linear interpolation) and is divided by two in divider 26. The resultant value is stored in correction table 27, for use when the same power level and frequency combination is next selected.

Correction table 27 has space for 12 x 21 values - i.e. twenty-one power levels at twelve different frequencies. There are, in fact 124 different frequency channels that can be selected, but it is considered necessary to store values for every tenth channel only. Each entry stores a power correction value to a resolution of 0.1dB. One bit of each entry represents the sign of the correction (i.e. indicating whether the previously measured power was over power or under power). Upon power-up, the table 27 will be empty and it will gradually fill up with correction values as the transmitter is operated at different power levels at different frequencies.

The divider 26 provides a damping factor, allowing the actual output power to approach the calibrated output power over a series of time slots at the particular power level, without "hunting".

The frequency correction value allows compensation for the fact that a given control voltage will not necessarily give rise to the same output power over the whole frequency range of the amplifier.

It will, of course, be understood that the frequency correction values 27 could be implemented by other means. For example, the values stored could be detector values, and the conversion to power values and division by 2 could be carried out upon read-out. A similar table may be provided for temperature correction, allowing correction values to be selected in response to temperature measured by a thermostat.

The invention has the advantage that re-calibration of the power amplifier is very simple in the field. If, for example, it is necessary to replace the power amplifier of a transmitter (as is often the case in the event of lightning strike), all that is necessary for re-calibration is that the field en-

gineer calibrates the replacement amplifier to the high power value. Thereafter, the microprocessor can enter a calibration routine which allows every other value for the control voltage at the calibration points to be determined automatically. In addition, means may be provided for receipt of a recalibration instruction, e.g. over the r.f. interface, or from a monitoring receiver, causing automatic initiation of the calibration program of steps (a) to (r).

Instead of the above described interpolation routine, an alternative method of ensuring that the start point for the calibration coincides with the finishing point is to repeat the calibration and at each stage replace the method of Figure 1a with that of Figure 1b (or vice versa) i.e., instead of using the 20dB pad to step the power down and then using the 2dB pad to step up in 10 incremental steps to return to the original point, the opposite can be done, stepping the power down in 2dB steps and, after 10 such steps, stepping up again in one 20dB step. When 10 calibration points have been derived by each method, the average point is taken between corresponding pairs from the two sets of points so derived.

Referring to Figure 4, further, preferred details of the attenuators 21 and 22, the switches 23 and 24 and the detector 14 of figure 2 are shown. It can be seen that switch 23 comprises two parts - 23a and 23b and switch 24 likewise comprises two parts - 24a and 24b. On either side of attenuator 21, there is a further switch 30a and 30b, and likewise there is a further switch, 31a and 31b, on either side of the attenuator 22. In addition to detector 14, there is a further detector 14' and the detectors 14 and 14' are applied to the + and - inputs of a comparator 32.

The purpose of the additional switches 30a, 30b, 31a and 31b is to isolate the attenuators 21 and 22 when they are short-circuited. This is necessary, because each attenuator comprises a T-network of resistors, with the stem of the T being connected to ground. For this reason, unless the attenuator is isolated, it still has a residual effect even when it is short circuited. Because the switches are not lossless switches, it is necessary to provide two switches in the short-circuit path (23a and 23b etc) in order to balance the corresponding switches 30a and 30b on either side of the attenuator 21.

The purpose of the additional detector 14' is for temperature compensation. The two detectors 14 and 14' are mounted in the same housing, in isothermal relationship, as is described in EP-A-0369135.

Referring to Figure 5, further details are shown of the switches and attenuator within the dotted line on Figure 4. From this figure, it can be seen that the switches 24a and 31a are implemented in the

surface-mount diode pair 50 and the switches 24b and 31b are implemented in a further diode pair 51. Various other resistors, capacitors and inductances are shown, which need not be described in detail, but which cause the diode pairs to act as switches in a manner known in the general art. It is a novel feature of the preferred embodiment of the invention that surface mount diode pair 51 is a mirror image of surface mount diode pair 50. This allows for a very compact arrangement of the components on a circuit board.

The provision of a first surface mount device comprising a first pair of diodes having a common electrode and a second surface mount device which is a mirror image of the first surface mount device has wider uses than just for the switching of attenuators.

Referring to Figure 6, an alternative arrangement for the 20dB pad 21, the switch 23 and the detector 14 is shown. In this alternative arrangement, a second detector 14b is provided in permanent serial connection with the 20dB pad 21. Instead of an open/closed switch 23, a two-way switch 23' is provided for selecting either the detector 14 or the detector and attenuator 14b and 21 for output power measurement. A power value measured by one detector is subsequently used to control the amplifier power under output power measurement by the other detector. Care must be taken to ensure that the two detectors have the same characteristic. The arrangement has the advantage of switching d.c. instead of a.c.

It will, of course, be understood that the above description has been given by way of example only, and that modifications can be made within the scope of the invention.

Claims

1. An amplifier comprising a controllable output power stage, power setting means for setting the output power, and a control loop for adjusting the output power, the control loop comprising measuring means for measuring the output power and comparison means for comparing the power measured with the power set and adjusting the output power in response thereto, characterised by attenuator means switchable into the control loop for causing the measuring means to measure attenuated power, storage means for storing a value for measured power and means for using a stored value derived from a first switched state of attenuation for adjustment of the output power during a second switched state of attenuation, thereby to allow a wide adjustment of output power over a narrow range of measured power.

2. An amplifier according to claim 1, wherein the

attenuator means comprises a large attenuator and a small attenuator and switching means for switching one or both of said attenuators into the control loop.

3. A method of controlling the output power of an amplifier, comprising the steps of:

- a) setting an output power stage to provide a desired higher output power, attenuating the output power in an attenuator, and measuring and storing a value for the attenuated output power
- b) deactivating the attenuator and
- c) adjusting the setting of the output power stage until substantially the same output power value is measured as the stored value, thereby providing a decreased output power, the value of which is controllable to substantially the same degree of accuracy as the measurement of the previously attenuated higher output power.

4. A method of controlling the output power of an amplifier, comprising the steps of:

- a) setting an output power stage to provide a desired lower output power, and measuring and storing a value for said output power,
- b) attenuating the output power in an attenuator
- c) adjusting the setting of the output power stage until substantially the same output power value is measured as the stored value, thereby providing an increased output power, the value of which is controllable to substantially the same degree of accuracy as the measurement of the previously set lower output power.

5. A method according to claim 3 or 4, further comprising the steps of attenuating the output power in large and small increments, and storing power values and corresponding output power stage settings which provide different output powers across a complete power range greater than one of said large increments, said different output powers being separated by amounts substantially equal to said small increments.

6. A method according to claim 5, wherein, by said means, the output power is set to different levels extending over a range by a series of steps including at least one large incremental step in one direction and a series of small incremental steps in the other direction so as to adjust the power back to the original level and, when the power has been adjusted over the whole range, a comparison is made between the original measured level and the final measured level and, by interpolation, the stored settings for the intermediate small incremental steps are adjusted so as to equalise the final level to the originally measured level.

7. A method of controlling the output power of an amplifier comprising the steps of obtaining a set of power settings separated by incremental steps by the method of claim 3 and a set of similar power settings separated by incremental steps by the

method of claim 4 and averaging corresponding values in the two sets.

8. A method according to any one of claim 5 to 7, wherein the method is executed automatically by the radio transmitter upon provision of an initial output power stage setting. 5

9. A method according to any one of claims 3 to 8, comprising the further steps of storing values representative of the measured and stored output values for different output power levels and frequencies and using those stored values for correction of the output power when those power levels and frequencies are next selected for output. 10

10. An amplifier substantially as hereinbefore described with reference to Figure 2. 15

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FIG. 1A

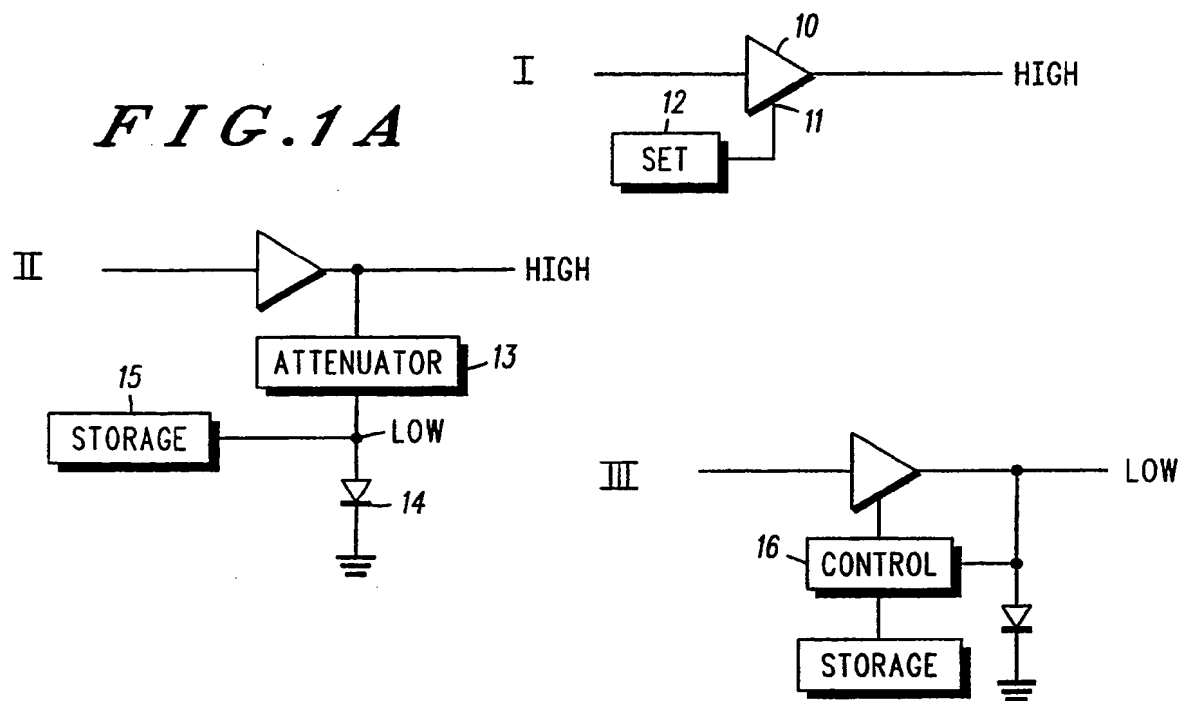
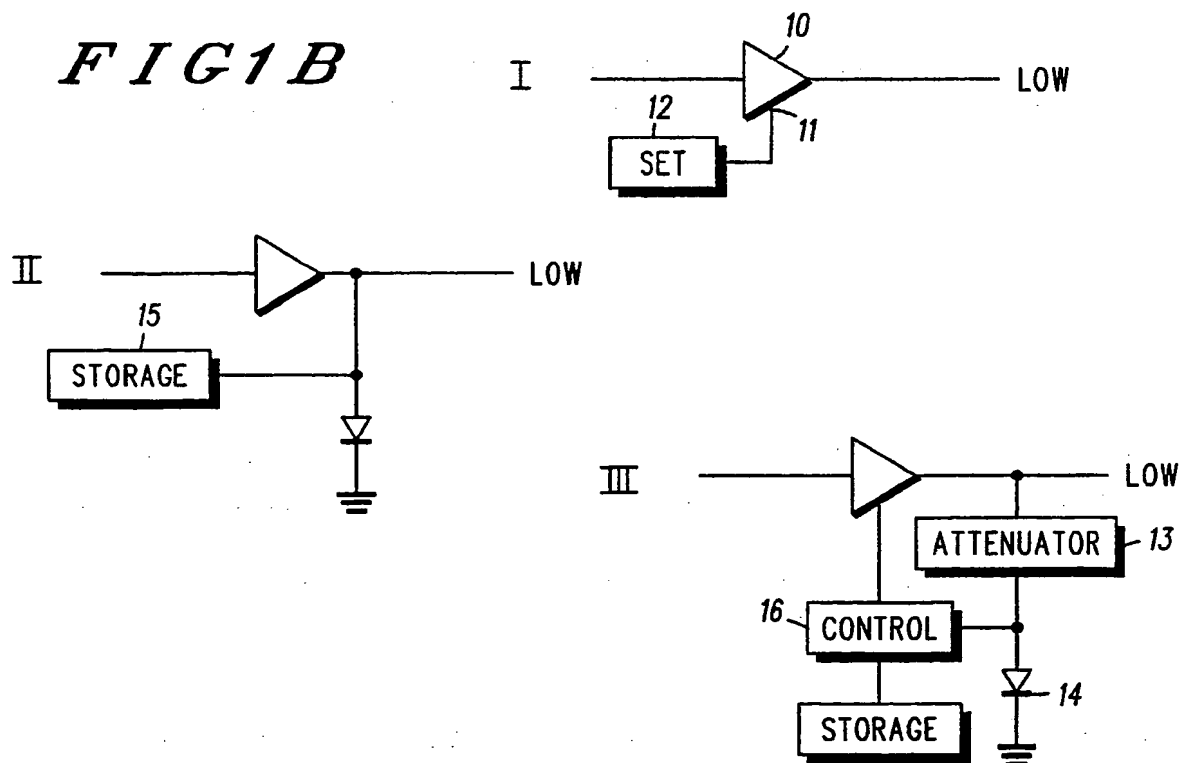


FIG 1B



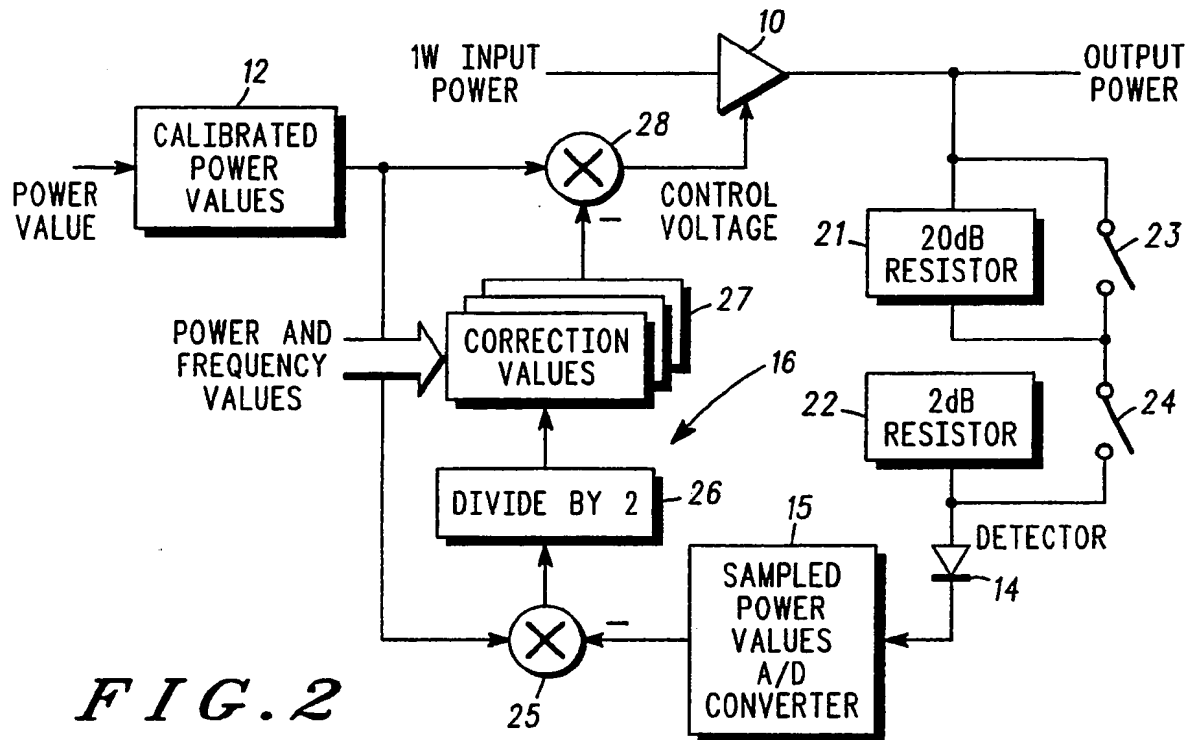


FIG. 2

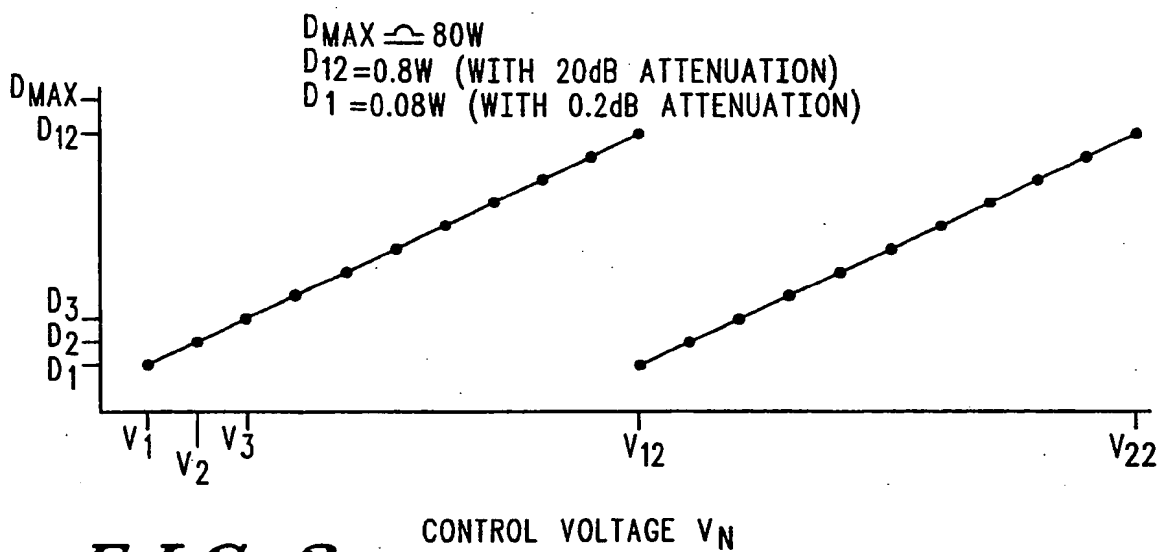
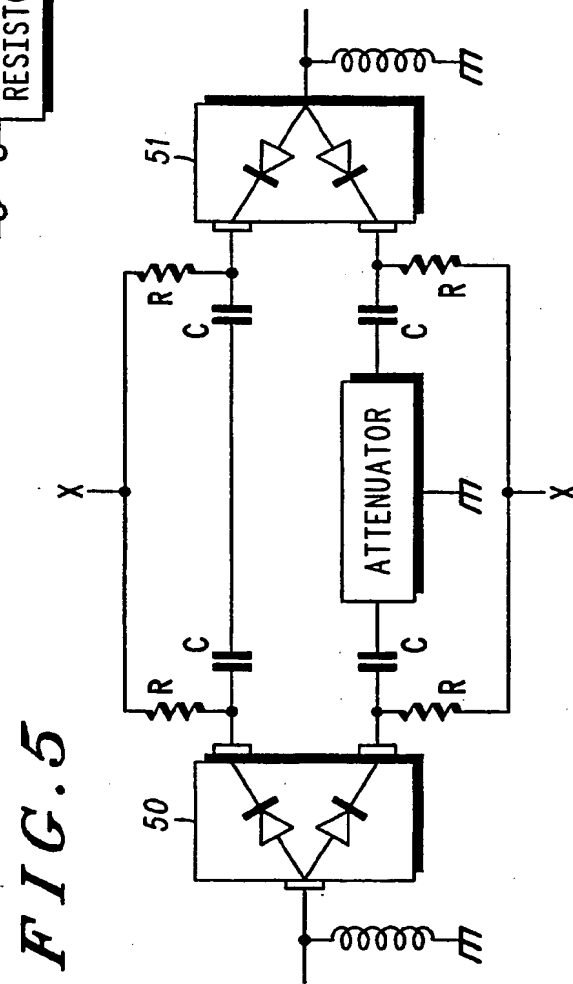
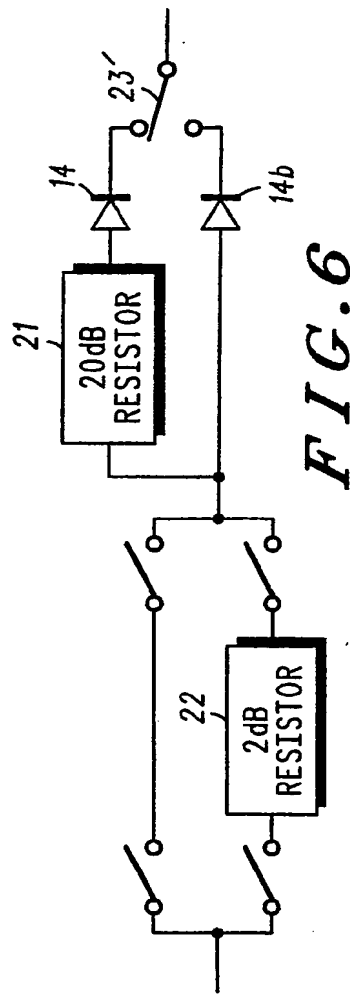
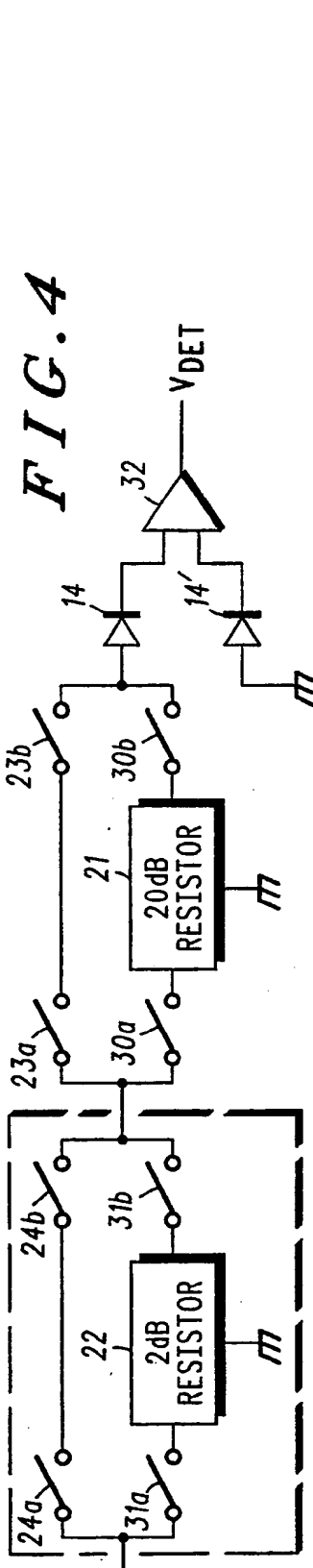


FIG. 3





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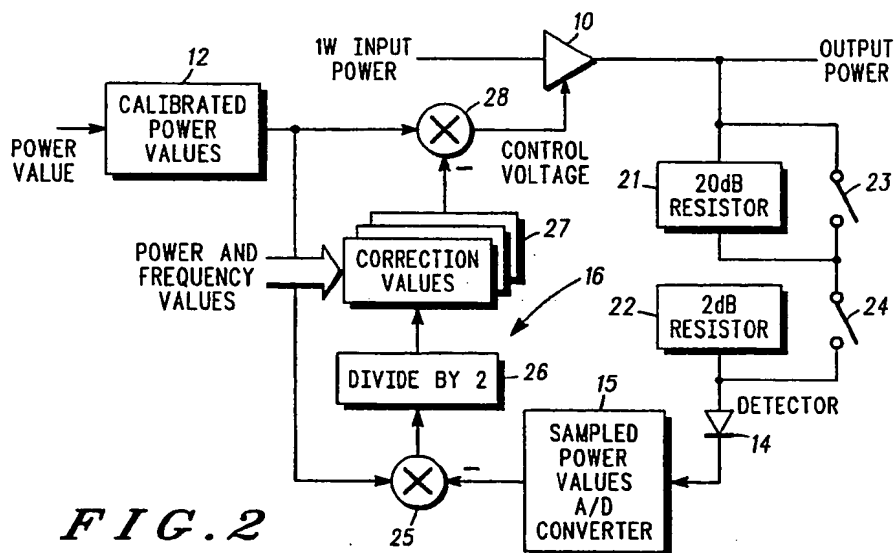


FIG. 2



European
Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 90 11 4596

DOCUMENTS CONSIDERED TO BE RELEVANT					
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)		
A	DE-A-3 527 554 (ROHDE & SCHWARZ) * Column 3, line 7 - column 4, line 22; figure * - - - -	1,3,4	H 03 G 3/20		
A	WO-A-8 607 216 (HUGHES AIRCRAFT CO.) * Page 4, line 32 - page 5, line 30 * - - - -	1,3,4			
D,P,A	EP-A-0 369 135 (MOTOROLA) * Column 2, lines 30-39; column 4, lines 35-51; figure 2 * - - - - -	1,3,4			
			TECHNICAL FIELDS SEARCHED (Int. Cl.5)		
			H 03 G H 04 Q		
The present search report has been drawn up for all claims					
Place of search The Hague		Date of completion of search 16 July 91	Examiner BLAAS D.-L.A.J.		
<table border="0"><tr><td>CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention</td><td>E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons ----- &: member of the same patent family, corresponding document</td></tr></table>				CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention	E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons ----- &: member of the same patent family, corresponding document
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